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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kevin Frazier, et al.
Serial No:	09/730,453
Filed:	December 5, 2000
For:	MULTI-PROTOCOL PACKET TRANSLATOR
Examiner:	Not yet assigned
Art Unit:	2661

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Commissioner for Patents, Washington, D.C. 20231, on the 25th day May, 2001.

M. Brad Lawrence, Reg. No. 47,210

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

In response to the NOTICE TO FILE CORRECTED APPLICATION PAPERS mailed March 14, 2001, please amend the above-identified application as follows:

In the Specification:

Please replace the paragraph beginning at line 1 of page 5 as shown.

FIG. 13 illustrates a next step in translating the packet of FIG. 7A into the packet of FIG. 7B, using the circuit of FIG. 10;

Please replace the paragraph beginning at line 3 of page 27 as shown.

FIG. 13 illustrates the next step in the translation. At this point, the two most significant bytes for the ElanID field are stored in a four byte word in the information memory 101b, as shown. These two bytes cannot be written directly to the output memory, however, because the output memory requires a four byte word to be written. Accordingly, the two bytes of the ElanID need to be stored in the storage alignment units 103, for later writing to the output memory 105. This is done as illustrated in FIG. 13. During this clock cycle, no information is

written to the output memory. Accordingly, the output memory continues to hold the same partially translated packet of FIG. 12B.

Please replace the paragraph beginning at line 11 of page 27 as shown.

At the step illustrated in FIG. 13, the other two pipelines hold two instructions that require reading of information from the input memory 100b -- jump orig B0 at 131a (which causes the input memory 100b to jump to an operand address -- to cause the address controller (not shown) of the input memory 100b to skip over the portions of the original packet header that are not used in the translated packet, i.e., fields 71, 72 of FIG. 7A). By changing the address of the input memory 100b, the next portion of the header to be read can be moved to an address that skips (deletes) fields 71, 72 of FIG. 7A (deletes the VDA, VSA and TAG type fields). In this particular embodiment, the read latency of the input memory 100b is longer than the read latency of the information memory 101b. When instructions involving reading of the input memory 100b reach the first stage 110 of the pipeline unit (at 131a and 131b), the control unit (not shown) causes the input memory's address control unit 100a to apply the applicable address and initiates a read of the input memory 100b.

REMARKS

In response to the NOTICE TO FILE CORRECTED APPLICATION PAPERS mailed March 14, 2001, Applicants respectfully assert that the drawings originally submitted are correct. However, minor typographical errors in the Specification may have given the United States Patent and Trademark Office, Initial Patent Examination Division, the impression that certain drawings were missing or mislabeled. In order to rectify the discrepancy between the Specification and the drawings, Applicants have made the above amendments to the Specification. In particular, all references to "FIG. 13A" have been replaced with "FIG. 13". These amendments are believed to conform the Specification to the drawings as originally submitted and to overcome the informality note in the NOTICE TO FILE CORRECTED APPLICATION PAPERS.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now comply with the requirements in the NOTICE TO FILE CORRECTED APPLICATION PAPERS. If the Examiner believes, after this amendment, that the application is still has informalities, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825

Respectfully submitted
Frazier, et al., Applicant(s)

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MARKED-UP SPECIFICATION

FIG. 13[A] illustrates a next step in translating the packet of FIG. 7A into the packet of FIG. 7B, using the circuit of FIG. 10;

FIG. 13[A] illustrates the next step in the translation. At this point, the two most significant bytes for the ElanID field are stored in a four byte word in the information memory 101b, as shown. These two bytes cannot be written directly to the output memory, however, because the output memory requires a four byte word to be written. Accordingly, the two bytes of the ElanID need to be stored in the storage alignment units 103, for later writing to the output memory 105. This is done as illustrated in FIG. 13[A]. During this clock cycle, no information is written to the output memory. Accordingly, the output memory continues to hold the same partially translated packet of FIG. 12B.

At the step illustrated in FIG. 13[A], the other two pipelines hold two instructions that require reading of information from the input memory 100b -- jump orig B0 at 131a (which causes the input memory 100b to jump to an operand address -- to cause the address controller (not shown) of the input memory 100b to skip over the portions of the original packet header that are not used in the translated packet, i.e., fields 71, 72 of FIG. 7A). By changing the address of the input memory 100b, the next portion of the header to be read can be moved to an address that skips (deletes) fields 71, 72 of FIG. 7A (deletes the VDA, VSA and TAG type fields). In this particular embodiment, the read latency of the input memory 100b is longer than the read latency of the information memory 101b. When instructions involving reading of the input memory 100b reach the first stage 110 of the pipeline unit (at 131a and 131b), the control unit (not shown) causes the input memory's address control unit 100a to apply the applicable address and initiates a read of the input memory 100b.